

06-19-00

A

LERNER AND GREENBERG, P.A.

PATENT ATTORNEYS AND ATTORNEYS AT LAW

2200 Hollywood Boulevard
Hollywood, Florida 33020
Tel: (954) 925-1100
Fax: (954) 925-1101

Herbert L. Lerner (NY Bar)
Laurence A. Greenberg (FL Bar)

Werner H. Stemer (FL Bar), Senior Attorney

Ralph E. Locher (FL, IL, MO Bars)
Manfred Beck (US & German Pat. Agent)
Mark P. Weichselbaum (TN Bar)
Gregory L. Mayback (FL Bar)
Markus Nollff (FL Bar)
Otto S. Kauder (Reg. Pat. Agent)
Loren Donald Pearson (FL Bar)

www.patentusa.com
patents@patentusa.com

Mailing Address:
Post Office Box 2480
Hollywood, FL 33022-2480

New York Office
153 E 57th Street
Suite 15G
New York, NY 10022

06/16/00
09/595860
U.S. PTO



"Express Mail" mailing label number EL080658350US
Date of Deposit June 16, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Docket No.: GR 97 P 6457


MICHAEL BURNS

Date: June 16, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : JÖRG BERTHOLD ET AL.
Title : INTEGRATED ELECTRICAL CIRCUIT AND METHOD FOR FABRICATING IT

2 sheets of formal drawings in triplicate.
A check in the amount of \$762.00 covering the filing fee.
Information Disclosure Statement and 8 References.
PCT Publication (cover sheet only).

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,


For Applicants
LAG:tg

LAURENCE A. GREENBERG
REG. NO. 29,308

06/16/00
U.S. PTO

06/16/00
09/595860
U.S. PTO

INTEGRATED ELECTRICAL CIRCUIT AND METHOD FOR FABRICATING IT

5 Cross-Reference to Related Application:

This is a continuation of copending International Application PCT/EP98/08255, filed December 16, 1998, which designated the United States.

10 Background of the Invention:

Field of the Invention:

The invention relates to an integrated electrical circuit having a plurality of structure planes, in which electrically active elements are situated on at least one element structure plane. At least one insulation layer is disposed above the element structure plane and electrical connecting leads are disposed within and/or above the insulation layer. At least a portion of the connecting leads contains so much copper that copper is predominant for the properties of the connecting leads, and at least one diffusion blocker is disposed underneath the connecting leads, which diffusion blocker impedes and/or prevents the diffusion of copper.

The invention furthermore relates to a method for fabricating such an integrated electrical circuit.

In integrated electrical circuits, an RC element is formed from the resistance of an interconnect and its capacitance, which depends on the material surrounding it and the geometry thereof. The attenuation and resonance effects of the RC

5 element adversely affect the signal propagation in the integrated electrical circuit. A diameter of the interconnect decreases considerably with the reduction of the feature sizes in the electrical circuit. Since, at the same time, the length of the interconnects is altered only slightly, the resistance of the interconnect increases. Therefore,
10 undesirable resonance and attenuation effects are increased in integrated electrical circuits with smaller feature sizes.

The use of copper as a material for the interconnect has been
15 proposed in order to solve this problem. Since copper has a higher electrical conductivity than aluminum, the resistance of the interconnect can thus be reduced.

When copper is used as a material for the interconnects,
20 however, the problem arises that the copper has to be prevented from diffusing into the structure plane in which the electrically active elements are situated. One reason for this is that copper atoms serve as centers for the production of charge carriers in a semiconductor substrate. A lifetime
25 of minority charge carriers is shortened by the generation of charge carriers. Moreover, the copper atoms act as seeds for

oxidation-induced stacking faults and weak points in thin oxide layers. The harmfulness of the copper to the electrically active elements contained in the element structure plane is intensified by a very high diffusion rate

5 of copper atoms in customary semiconductor materials - such as silicon. On account of the high diffusion rate, the copper atoms can diffuse through the entire semiconductor substrate at process temperatures usually starting from 400° Celsius. Therefore, irrespective of the point at which they pass into
10 the semiconductor material, the copper atoms can readily reach the critical points at which they initiate the undesirable consequential effects mentioned above.

One solution to the problem of copper diffusion is known from
15 the generic integrated electrical circuit described in the article titled "Barrier Metal Free Copper Damascence Interconnection Technology Using Atmospheric Copper Reflow and Nitrogen Doping in SiOF Film", K. Mikagi, et al., IEDM 1996, pp. 365-368. The article furthermore discloses a method for
20 fabricating the integrated electrical circuit. In that case, a thin diffusion blocker is disposed directly underneath an interconnect composed of copper. The diffusion blocker is formed as follows. First a trench for accommodating the interconnect composed of copper is etched into the insulation
25 layer. The surface of the patterned insulation layer composed of SiOF is subsequently converted superficially into SiON by

nitriding in an NH_3 plasma. This makes it possible for the interconnect to be composed of copper in its entire cross section. The thickness of the layer serving as a diffusion blocker is small and amounts to a few nm. The barrier effect
5 of such a layer is limited. The circuit has the disadvantage that the diffusion of copper is not reliably stopped.

Furthermore, it is known to connect different structure planes of an electrical circuit with contact holes filled with
10 copper. In that case, the copper is enclosed on all sides by a diffusion-inhibiting barrier layer. The barrier layer has a minimum layer thickness for preventing copper from diffusing into the substrate in which it is situated. In order to effectively prevent the diffusion, the barrier layer must not
15 fall below a certain thickness. A barrier layer thickness sufficient to prevent diffusion leads to only a small portion of the interconnect cross section being composed of copper. Since all known barrier layers have a considerably higher resistivity than copper, the effective electrical conductivity
20 thus decreases undesirably with the progressive decrease in the width of the contact holes.

Summary of the Invention:

It is accordingly an object of the invention to provide an
25 integrated electrical circuit and a method for fabricating it that overcome the above-mentioned disadvantages of the prior

art devices and methods of this general type, in which as far as possible undisturbed current conduction is obtained even with small feature sizes. Resonance and attenuation effects should be as minor as possible even at a high signal

5 frequency. Furthermore, the intention is to effectively prevent copper atoms from diffusing into the semiconductor substrate.

With the foregoing and other objects in view there is

10 provided, in accordance with the invention, an integrated electrical circuit, including:

a plurality of structure planes including at least one element structure plane;

15 electrically active elements disposed on the at least one element structure plane;

at least one insulation layer disposed above the at least one

20 element structure plane;

electrical connecting leads disposed at least one of within and above the insulation layer, at least a portion of the electrical connecting leads contain copper;

25

connection pieces disposed underneath the electrical connecting leads; and

at least one diffusion blocker disposed underneath the
5 electrical connecting leads, the diffusion blocker impedes and/or prevents a diffusion of copper, the diffusion blocker is configured as a blocker layer interrupted only in a region having contact holes formed therein and/or in a region of the connection pieces, the blocker layer is disposed between the
10 at least one element structure plane and the insulation layer.

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217

layer. The diffusion barrier can be realized by filling the contact holes with a conductive material that has a diffusion barrier effect for copper. The material may be, in particular, tungsten or titanium nitride. Furthermore, the

5 diffusion barrier may be realized by a thin layer which lines the side walls and the bottom of the contact hole and exhibits the diffusion barrier effect for copper. In particular, titanium/titanium nitride, titanium nitride, tantalum nitride or the like is suitable for the thin layer. The thin layer

10 may be realized by an adhesion layer of the kind frequently used when contact holes are filled with tungsten. The thin layer has a thickness of 50 to 200 nm, preferably of 50 to 100 nm. The diffusion barrier at the surface of the contact holes forms, together with the blocker layer, a continuous

15 layer with a diffusion barrier effect against copper. This effectively prevents copper atoms from passing into the semiconductor substrate. The copper-containing connecting lead is isolated from the semiconductor substrate by a closed diffusion barrier layer formed from the blocker layer and the

20 diffusion barrier which is effective at the surface of the contact holes.

The connecting leads may be both interconnects and electrical contacts.

The interconnects preferably extend within a structure plane and serve to connect different active electrical elements to one another or to contacts located outside the actual integrated electrical circuit. They may be part of a totality of layers made of conductive and insulating materials, the layers being constructed above the active elements and being multiply patterned laterally. This totality is also referred to as a metalization layer.

Connecting leads serving as direct electrical contacts are preferably formed by contact holes filled with a conductive material. The contact holes preferably extend perpendicularly to the structure planes from which the integrated electrical circuit is constructed.

The connecting leads contain so much copper that copper is predominant for the properties of the connecting leads. In this case, it is possible, in principle, for the connecting leads to be composed completely of copper. However, it is likewise possible for the connecting leads to be formed from a material which contains copper only as a proportion and furthermore has additions for example of zirconium, hafnium or the like. However, according to the invention this proportion is so large that the copper is present in a content that suffices for considerably increasing the electrical conductivity of the material. To that end, it is expedient

for the copper content in the connecting leads to be at least 10 percent by weight. In this case, copper is present in a concentration which is higher than that required to improve the process properties of the method for fabricating an

5 interconnect, with the result that the properties, in particular the electrical conductivity, the etching behavior, the adhesion, the seeding, the deposition properties, the surface properties and the like, of the connecting leads are determined by the copper. Copper-specific processes may be necessary, therefore, during the fabrication of the connecting leads. In order to exhaust the potential of the copper-containing connecting leads, it is advantageous to provide a copper content of greater than or equal to 90 percent by weight in the connecting leads.

15 A diffusion blocker is situated underneath the connecting leads. However, at least one insulation layer is disposed between the connecting leads and the diffusion blocker.

20 The insulation layer may be constructed from any desired material. In order to obtain the smallest possible RC constant of the connecting lead, however, it is expedient for the dielectric constant of the material used for the insulation layer to be as small as possible. The smallest possible dielectric constant of the insulation layer can be
25 obtained when the latter is composed of air or an aerogel.

However, materials that can be integrated more easily in the fabrication process also have a suitable, small dielectric constant. Examples of these materials that may be mentioned are semiconductor oxides such as SiO_2 , semiconductor nitrides such as Si_3N_4 , fluorinated semiconductor oxides such as SiOF , fluorinated (amorphous) carbon, nitrides such as boron nitride, polymers and polymer compounds such as polyimides, in particular fluorinated polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, fluoropolymers such as tetrafluoroethylene.

The blocker layer is situated underneath the insulation layer. Therefore, the blocker layer is spatially separated from the connecting leads. The consequence of this configuration is that copper atoms can penetrate into the insulation layer. The invention does not, therefore, preclude partial penetration of individual copper atoms into the insulation layer. It has been shown that such minor penetration of copper atoms into the insulation layer does not adversely affect the functionality of the integrated electrical circuit.

The blocker layer serving as a diffusion blocker can, in principle, be formed from any material. A material which, at the customary process temperatures of, as a rule, in excess of 400 degrees Celsius, has a diffusion length for copper which

is less than the thickness of the blocker layer is expediently used.

It is particularly advantageous for the blocker layer to
5 contain nitrogen, oxygen, fluorine or a compound of these elements.

Examples of suitable materials for the blocker layer are
nitrides such as silicon nitride Si_3N_4 , oxidized nitrides such
10 as, for example, silicon oxynitride SiON , silicon boron
oxynitride SiBON , TiN_xO_y , TaN_xO_y , WN_xO_y , WSi_xN , fluorinated
nitrides such as silicon fluorooxynitride SiOFN , and also
metal oxides such as TiO_2 , Ta_2O_5 .

15 It is particularly expedient for the thickness of the blocker
layer to be between 50 nm and 800 nm.

A minimum layer thickness of approximately 100 nm suffices in
the majority of cases to effectively prevent copper atoms from
20 diffusing into the plane of the electrically active elements.
A possible upper limit for the layer thickness is provided by
the intention of avoiding an undesirable increase in the
lateral coupling capacitances and also an unfavorable
geometrical shape of the insulation layer.

The invention also includes the case where a plurality of blocker layers are provided. The blocker layers may be situated on different structure planes and the extent to which they impede diffusion or prevent diffusion may differ.

5

It is likewise expedient for at least one further diffusion blocker to bear on at least a portion of the connecting leads.

10

The further diffusion blocker may be shaped as desired. It is particularly advantageous, however, for the further diffusion blocker to bear on the side areas and/or the lower edges of at least a portion of the connecting leads. This portion of the connecting leads may involve both the interconnects and the electrical contacts.

15

It is expedient to configure the further diffusion blocker or blockers in such a way that they prevent bulk outdiffusion of the copper into the insulation layer, and that the blocker layer impedes diffusion to a greater extent.

20

This configuration can be obtained in a particularly simple and expedient manner by the blocker layer being thicker than the further diffusion blocker.

In an alternative, a diffusion through the blocker layer is less than 10% of the diffusion through the further diffusion blocker.

- 5 The invention furthermore relates to a method for fabricating an integrated electrical circuit, the method includes:

forming electrically active elements in a region of a surface of a semiconductor substrate,

10

applying an insulation layer on the electrically active elements,

15

producing electrical connecting leads, which contain so much copper that copper is predominant for the properties of the connecting leads, within and/or on the insulation layer, and

applying at least one diffusion blocker underneath the connecting leads.

20

According to the invention, the method is carried out in such a way that before the insulation layer is produced, the diffusion blocker is deposited as a continuous blocker layer, and that the insulation layer is produced on the blocker

25 layer.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in an integrated electrical circuit and a method for fabricating it, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

10
15
20
25

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic, cross-sectional view through an integrated electrical circuit having a blocker layer which is interrupted by contact holes filled with tungsten according to the invention;

Fig. 2 is a detailed sectional view from Fig. 1 in a region of a filled contact hole;

Fig. 3 is a sectional view of a second embodiment of the integrated electrical circuit having the blocker layer which is interrupted by the tungsten-filled contact holes and the connection pieces; and

5

Fig. 4 is a sectional view of a detail shown in Fig. 3 in the region of the contact hole.

Description of the Preferred Embodiments:

10 In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an integrated electrical circuit having field-effect transistors 20, 30 and 40 that are situated on a
15 semiconductor substrate 10 preferably composed of silicon. The field-effect transistors 20, 30 and 40 each have source and drain regions 50, 60, 70, 80, 90 and 100 and also gate electrodes 120, 130 and 140.

20

An insulation layer 150 is situated between the field-effect transistors 20, 30 and 40 and also above the source and drain regions 50, 60, 70, 80, 90 and 100 and also between the gate electrodes 120, 130 and 140. The insulation layer 150 may be
25 formed, in particular, by an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate

glass (BPSG). The intermediate oxide can be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

A blocker layer 160 having a thickness of 150 nm and made, for example, of silicon oxynitride SiON is disposed above the insulation layer 150. The blocker layer 160 is disposed above the entire surface of the semiconductor substrate 10 and is interrupted only in a region of contact holes 170, 180, 190, 200, 210 and 220. The contact holes 170, 180, 190, 200, 210 and 220 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy.

As can be discerned from Fig. 2, an adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between a tungsten filling 230 of a contact hole 240 and the layers which bound the contact hole, that is to say the insulation layer 150 and the blocker layer 160. The adhesion layer 165 serves as a seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 170, 180, 190, 200, 210, 220 and 240 with tungsten, for example. In

addition, the adhesion layer 165 protects the material underneath the bottom of the contact hole.

Above the contact holes 170, 180, 190, 200, 210, 220 and 240, connection pieces 250, 260, 270, 280, 290, 300 and 310 are situated directly on the blocker layer 160. The connection pieces being made of a material which combines a high conductivity with a minor diffusion tendency, for example aluminum.

10

A further insulation layer 320, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 250, 260, 270, 280, 290, 300 and 310.

15

However, it is not necessary for the insulation layer 320 to be composed of an oxide, although it is technologically particularly expedient for it to be composed of a

20

semiconductor oxide such as, for example, SiO_2 formed by a TEOS (tetraethyl orthosilicate = $\text{SiO}(\text{OC}_2\text{H}_5)_4$) method. As an alternative, it is possible for the insulation layer 320 (that is to say the intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases mentioned, the production of the insulation layer 320 can be integrated without difficulty in the process for fabricating the electrical circuit.

25

Contact holes 330, 340, 350, 360 and 370 are likewise etched into the insulation layer 320.

5 The contact holes 330, 340, 350, 360 and 370 are filled with tungsten or copper in a whole-area manner. Above the insulation layer 320, connection pieces 390 and 400 and also an interconnect 410 made of copper are situated in a further insulation layer 380.

10 Contact holes 420 and 430 are likewise situated in the insulation layer 380 and are in turn filled with tungsten or copper in a whole-area manner.

15 Connection pieces 440 and 450 made of copper are likewise disposed above the contact holes 420 and 430. The connection pieces 440, 450 are situated in an intermetal dielectric 460 which lies above the insulation layer 380 and is composed of a silicon oxide SiO_2 , for example.

20 The integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 20, 30 and 40 with the source and drain regions 50, 60, 70, 80, 90 and 100 and also with the gate electrodes 120, 130 and 140 are fabricated in a known manner in the region of a main
25 area of the semiconductor substrate 10.

This is followed by the production of the insulation layer 150, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

The blocker layer 160 having a thickness of approximately 100 nm is coated onto the insulation layer 150. The blocker layer 160 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane (SiH₄), ammonia (NH₃) and oxygen are used for carrying out the method. The blocker layer 160 is deposited at a pressure in the range of from about 20 to 100 Pa, preferably approximately 30 Pa, and a temperature below 500° C, preferably about 300° C.

20

Afterwards, the contact holes 170, 180, 190, 200, 210, 220 and 240 are etched into the insulation layer 150 and into the blocker layer 160, preferably by a dry etching method in a reactive plasma. An example of an etchant used is a gas mixture comprising CHF₃ and O₂ or containing CHF₃ and CF₄.

The adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 170, 180, 190, 200, 210, 220 and 240 are thereupon filled with tungsten or copper.

5

The connection pieces 250, 260, 270, 280, 290, 300 and 310 that may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer.

10

A patterning process according to a conventional photolithographic method patterns that part of the adhesion layer 165 which lies above the blocker layer 160 and equally the connection pieces 250, 260, 270, 280, 290, 300 and 310.

15

The insulation layer 320 is then deposited onto the blocker layer 160 and the connection pieces 250, 260, 270, 280, 290, 300 and 310 by a suitable deposition method - such as plasma enhanced chemical vapor deposition (PECVD).

20

The contact holes 330, 340, 350, 360 and 370 are then etched into the insulation layer 320 preferably by a dry etching method in a reactive plasma. An example of a suitable etchant used is a gas mixture containing CHF_3 and O_2 or containing CHF_3 and CF_4 .

25

The connection pieces 390 and 400 made of copper and also an interconnect 410, which serves for connecting the contact holes 350 and 360 and is likewise composed of copper, are produced in the manner explained below. A copper layer having
5 a thickness of from 300 nm to 600 nm is applied to the layer 320 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

The insulation layer 380 is subsequently applied. The contact
10 holes 420 and 430 are then etched into the insulation layer 380 preferably by a dry etching method in a reactive plasma. An example of an etchant used is once again a gas mixture containing CHF_3 and O_2 or containing CHF_3 and CF_4 . The contact
15 holes 420 and 430 are subsequently filled with copper. The connection pieces 440 and 450 made of copper are then applied to the contact holes 420 and 430.

A further plane 460 formed for example by an intermetal dielectric such as SiO_2 is subsequently applied.

20

In the case of a second embodiment of the integrated electrical circuit illustrated in Fig. 3, field-effect transistors 520, 530 and 540 are situated on a semiconductor substrate 510 preferably composed of silicon. The field-
25 effect transistors 520, 530 and 540 each have source and drain

regions 550, 560, 570, 580, 590 and 600 and also gate electrodes 620, 630 and 640.

An insulation layer 650 is situated between the field-effect transistors 520, 530 and 540 and also above the source and drain regions and also the gate electrodes. The insulation layer 650 may be composed, in particular, of an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate glass (BPSG). The intermediate oxide may be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

A blocker layer 660 having a thickness of 150 nm and made of silicon oxynitride SiON is disposed above the insulation layer 650. The blocker layer 660 is disposed above the entire surface of the semiconductor substrate 510 and encloses the connection pieces 750, 760, 770, 780, 790 and 800 located in the region of contact holes 670, 680, 690, 700, 710, 720 and 740. The contact holes 670, 680, 690, 700, 710 and 720 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy. The connection pieces 750, 760, 770, 780, 790, 800 and 810 are composed of a material that combines a

high conductivity with a minor diffusion tendency, for example aluminum.

As can be discerned from Fig. 4, an adhesion layer 665 having
5 a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between the tungsten filling 730 of a contact hole 740 and the layer which bounds the contact hole, that is to say in this case the insulation layer 650. The adhesion layer 665 serves as a
10 seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 670, 680, 690, 700, 710, 720 and 740 with tungsten, for example. In addition, the adhesion layer 665 protects the material underneath the bottom of the contact hole.

15 A further insulation layer 820, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 750, 760, 770, 780, 790, 800. However, it is not necessary for the insulation layer 820 to be composed
20 of an oxide, although it is technologically particularly expedient for it to be composed of a semiconductor oxide such as, for example, SiO_2 formed by a TEOS (tetraethyl orthosilicate = $\text{SiO}(\text{OC}_2\text{H}_5)_4$) method. As an alternative, it is possible for the insulation layer 820 (that is to say the
25 intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases

mentioned, the production of the insulation layer 820 can be integrated without difficulty in the process for fabricating the electrical circuit.

- 5 Contact holes 830, 840, 850 and 860 are likewise etched into the insulation layer 820.

The contact holes 830, 840, 850 and 860 are filled with tungsten or copper in a whole-area manner. Above the

- 10 insulation layer 820, connection pieces 890 and 890 and also an interconnect 910 made of copper are situated in a further insulation layer 880.

- 15 Contact holes 920 and 930 are likewise situated in the insulation layer 880 and are in turn filled with tungsten or copper in a whole-area manner.

Connection pieces 940 and 950 made of copper are likewise disposed above the contact holes 920 and 930.

20

- An integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 520, 530 and 540 with the source and drain regions 550, 560, 570, 580, 590 and 600 and also with the gate electrodes 620, 25 630 and 640 are fabricated in a known manner in the region of a main area of a semiconductor substrate 510.

This is followed by the production of the insulation layer 650, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a
5 coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

Afterwards, the contact holes 670, 680, 690, 700, 710, 720 and 740 are etched into the insulation layer 650, preferably by a
10 dry etching method in a reactive plasma. An example of an etchant used is a gas mixture containing CHF_3 and O_2 or containing CHF_3 and CF_4 .

The adhesion layer 665 having a thickness of approximately
15 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 670, 680, 690, 700, 710, 720 and 740 are thereupon filled with tungsten or copper.

The connection pieces 750, 760, 770, 780, 790 and 800, which
20 may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer made of aluminium or an aluminium alloy, for example. A patterning process according to a conventional
photolithographic method patterns that part of the adhesion
25 layer 665 which lies above the insulation layer 650 and equally the connection pieces 750, 760, 770, 780, 790 and 800.

The blocker layer 660 having a thickness of approximately 100 nm is then coated onto the insulation layer 650 and the connection pieces 750, 760, 770, 780, 790 and 800. The

5 blocker layer 660 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are
10 silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane (SiH_4), ammonia (NH_3) and oxygen are used for carrying out the method. The blocker layer 660 is preferably deposited at a pressure in the range of about 20 to 100 Pa, ideally at about 30 Pa, and a temperature of below
15 500° C, preferably about 300° C.

The connection pieces 750, 760, 770, 780, 790 and 800 are subsequently produced by applying and subsequently patterning a metal layer. The insulation layer 820 is then deposited
20 onto the blocker layer 660 and the connection pieces 750, 760, 770, 780, 790, 800 and 810 by a suitable deposition method such as chemical vapor deposition (CVD). The contact holes 830, 840, 850, 860 and 870 are then etched into the insulation layer 820. An example of an etchant used is a gas mixture
25 containing CHF_3 and O_2 or containing CHF_3 and CF_4 .

The connection pieces 890 and 900 made of copper and also an interconnect 910, which serves for connecting the contact holes 850 and 860 and is likewise composed of copper, are produced in the manner explained below. A copper layer having
5 a thickness of from 300 nm to 600 nm is applied to the insulation layer 820 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

The further insulation layer 880 is then deposited. The
10 contact holes 920 and 930 are then etched into the insulation layer 880 preferably by a dry etching method in a reactive plasma. An example of an etchant used is again a gas mixture containing CHF_3 and O_2 or containing CHF_3 and CF_4 . The contact holes 920 and 930 are subsequently filled with copper.
15 Connection pieces 940 and 950 made of copper are then applied to the contact holes 920 and 930.

The intermetal dielectric 960, for example made of silicon oxide SiO_2 , is subsequently applied.

We claim:

1. An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

at least one insulation layer disposed above said at least one element structure plane;

electrical connecting leads disposed at least one of within and above said insulation layer, at least a portion of said electrical connecting leads contain copper;

connection pieces disposed underneath said electrical connecting leads; and

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impedes and prevents a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker

layer disposed between said at least one element structure plane and said insulation layer.

2. The integrated electrical circuit according to claim 1, including a diffusion barrier for impeding a diffusion of copper disposed at at least one of a surface of said contact holes and said connection pieces.

3. The integrated electrical circuit according to claim 1, wherein said electrical connecting leads have a copper content that is at least 10 percent by weight.

4. The integrated electrical circuit according to claim 1, wherein said insulation layer contains at least one substance selected from the group consisting of semiconductor oxides, semiconductor nitrides, fluorinated semiconductor oxides, fluorinated (amorphous) carbon, nitrides including boron nitride, polymers and polymer compounds including polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, and fluoropolymers.

5. The integrated electrical circuit according to claim 1, wherein said blocker layer contains one of nitrogen, oxygen, fluorine, and a compound thereof.

6. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a nitride.

7. The integrated electrical circuit according to claim 6, wherein said blocker layer contains one of silicon nitride Si_3N_4 and tungsten silicon nitride WSi_xN .

8. The integrated electrical circuit according to claim 5, wherein said blocker layer contains an oxidized nitride.

9. The integrated electrical circuit according to claim 8, wherein said blocker layer contains at least one compound selected from the group consisting of silicon oxynitride SiON , silicon boron oxynitride SiBON , titanium oxynitride TiN_xO_y , tantalum oxynitride TaN_xO_y , and tungsten oxynitride WN_xO_y .

10. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a fluorinated nitride.

11. The integrated electrical circuit as claimed in claim 10, wherein said blocker layer contains silicon fluorooxynitride SiOFN .

12. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a metal oxide.

13. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a material selected from the group consisting of titanium oxide TiO_2 and tantalum oxide Ta_2O_5 .

14. The integrated electrical circuit according to claim 1, wherein said blocker layer has a thickness of between 50 nm and 800 nm.

15. The integrated electrical circuit according to claim 1, wherein said blocker layer is one of a plurality of blocker layers.

16. The integrated electrical circuit according to claim 15, wherein said blocker layers are disposed on different ones of said structure planes.

17. The integrated electrical circuit according to claim 15, wherein an extent to which said blocker layers impede diffusion and prevent diffusion differs.

18. The integrated electrical circuit according to claim 1, including at least one further diffusion blocker bearing on at least a portion of said electrical connecting leads.

19. The integrated electrical circuit according to claim 18,

wherein said further diffusion blocker bears on at least one of side areas and lower edges of said portion of said electrical connecting leads.

20. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker prevents bulk outdiffusion of copper into said insulation layer.

21. The integrated electrical circuit according to claim 18, wherein an extent to which said blocker layer impedes diffusion is greater than that of said further diffusion blocker.

22. The integrated electrical circuit according to claim 18, wherein said blocker layer has a thickness greater than that of said further diffusion blocker.

23. The integrated electrical circuit according to claim 18, wherein a diffusion through said blocker layer is less than 10% of a diffusion through said further diffusion blocker.

24. A method for fabricating an integrated electrical circuit, which comprises:

forming electrically active elements in a region of a surface of a semiconductor substrate;

applying at least one diffusion blocker as a continuous blocker layer on the electrically active elements;

subsequently, applying at least one insulation layer on the continuous blocker layer; and

forming copper-containing electrical connecting leads at least one of within and on the insulation layer.

04931028600

Abstract of the Disclosure:

An integrated electrical circuit having a plurality of structure planes is described. Electrically active elements are situated on at least one element structure plane, where at least one insulation layer is disposed above the element structure plane. Electrical connecting leads are disposed within and/or above the insulation layer, where at least a portion of the connecting leads contain copper. At least one diffusion blocker is disposed underneath the connecting leads, which diffusion blocker impedes and/or prevents the diffusion of copper. The integrated electrical circuit is configured according to the invention such that the diffusion blocker is configured as a blocker layer which is interrupted only in the region of contact holes and/or connection pieces and that the blocker layer is situated between the element structure plane and the insulation layer.

REL/kc

FIG 1

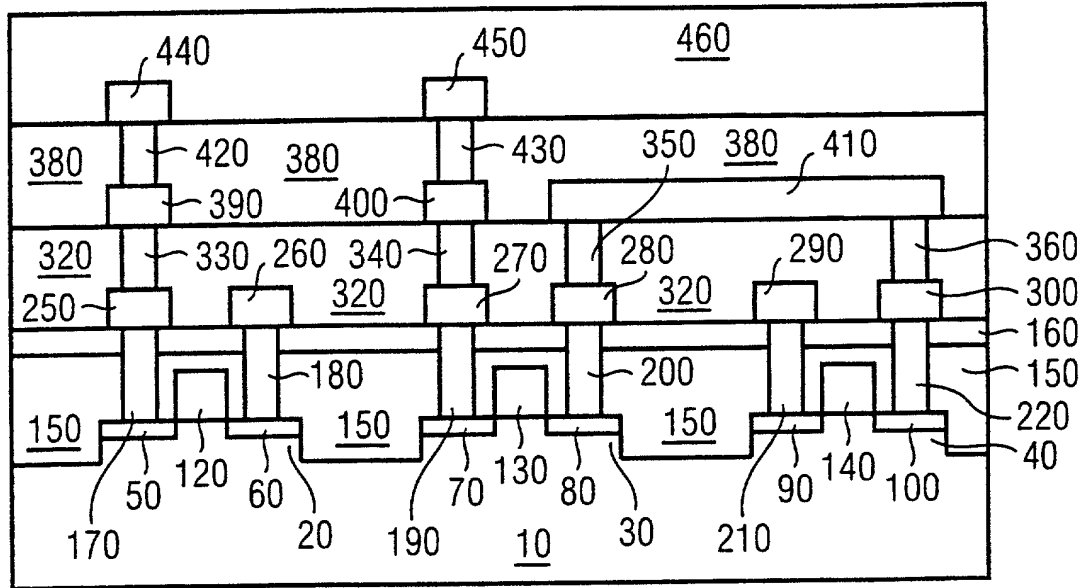


FIG 2

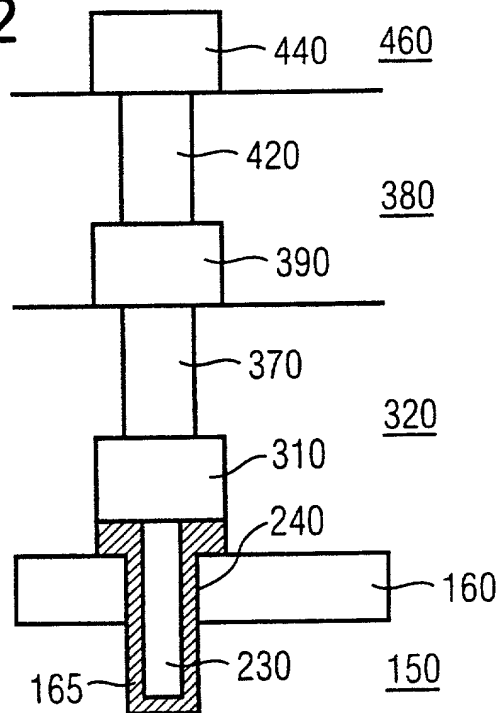


FIG 3

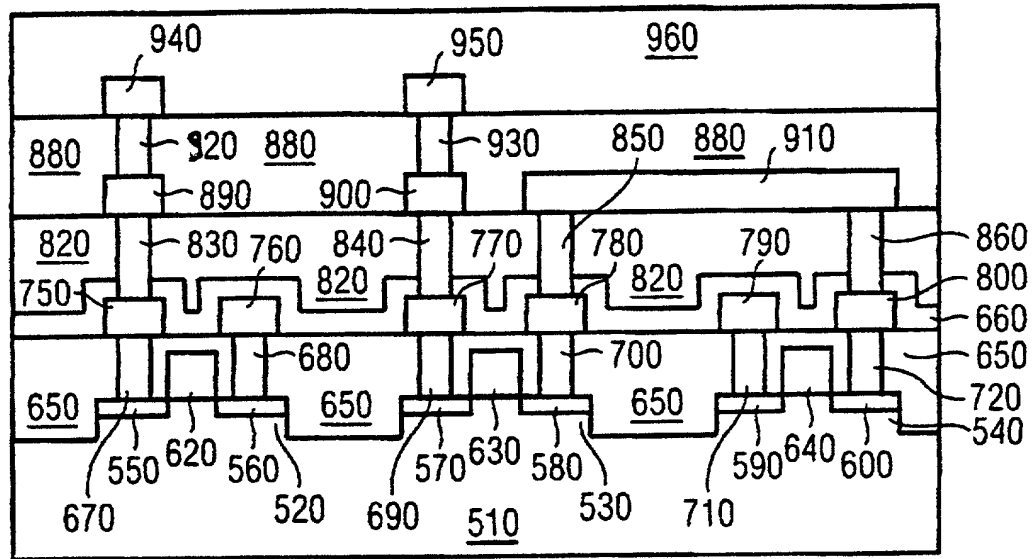
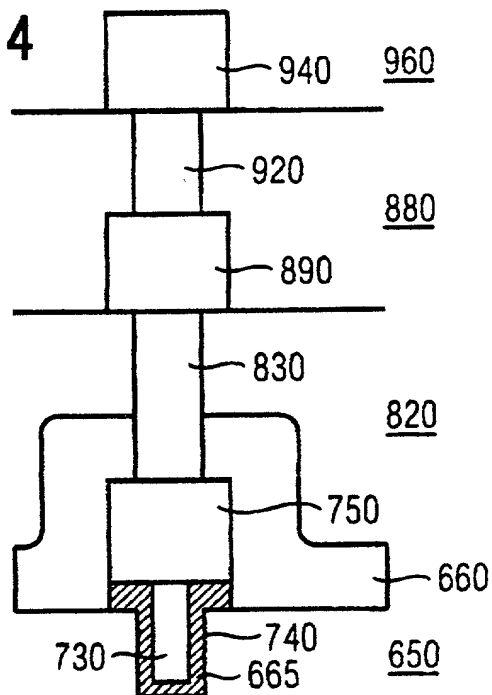


FIG 4



COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATED ELECTRICAL CIRCUIT AND METHOD FOR FABRICATING IT

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 197 55 869.0 filed December 16, 1997, the International Priority of which is claimed under 35 U.S.C. §119; and International Application No. PCT/EP98/08255, filed December 16, 1998, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

HERBERT L. LERNER (Reg.No.20,435)
LAURENCE A. GREENBERG (Reg.No.29,308)
WERNER H. STEMER (Reg.No.34,956)
RALPH E. LOCHER (Reg.No. 41,947)

Address all correspondence and telephone calls to:

LERNER AND GREENBERG, P.A.
POST OFFICE BOX 2480
HOLLYWOOD, FLORIDA 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST JOINT INVENTOR: JÖRG BERTHOLD

INVENTOR'S SIGNATURE: _____

DATE: _____

Residence: MÜNCHEN, GERMANY

Country of Citizenship: GERMANY

Post Office Address: EINSTEINSTRASSE 46,
D-81675 MÜNCHEN
GERMANY

FULL NAME OF SECOND JOINT INVENTOR: SIEGFRIED SCHWARZL

INVENTOR'S SIGNATURE: _____

DATE: _____

Residence: NEUBIBERG, GERMANY

Country of Citizenship: GERMANY

Post Office Address: JOSEF-KYREIN-STRASSE 11B,
D-85579 NEUBIBERG
GERMANY